AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An interconnect structure, comprising:

a plurality of interconnected nodes, including ~~distinct nodes A and E~~ a first node and a second node;

the first node [[A]] having a plurality of data input ports, a plurality of data output ports, and a control signal input port; and

the second node [[E]] having a plurality of data input ports, a plurality of data output ports, and a control signal output port; and

a routing logic associated with the nodes, the routing logic for routing data selectively among the interconnected nodes;

the first and second nodes ~~A and E~~ being positioned in the interconnect structure so that the first node [[A]] cannot route data to the second node [[E]], the second node [[E]] cannot route data to the first node [[A]], and no node exists in the interconnect structure that can have data routed directly to it from both the first node [[A]] and the second node [[E]]; and

a logic included as part of said routing logic and associated with the first node [[A]] that uses information concerning routing of data through the second node [[E]] to route data through the first node; [[A]]

wherein at least one of the plurality of nodes is adapted to simultaneously receive a plurality of messages.

2. (Currently Amended) An interconnect structure in accordance with Claim 1 wherein:

the plurality of interconnected nodes includes a third node [[F]] distinct from the first and second nodes ~~A and E~~, the third node [[F]] having a plurality of data input ports, a plurality of data output ports, and a control signal output port; and

the first and third nodes ~~A and F~~ are positioned in the interconnect structure so that the first node [[A]] cannot route data to the third node [[F]], the third node [[F]] cannot route data through the first node [[A]], and no node exists in the interconnect structure that can receive data directly routed both from the first node [[A]] and the third node [[F]]; and

the logic associated with the first node [[A]] uses information concerning routing of data through the third node [[F]] to route data through the first node [[A]].

3. (Currently Amended) An interconnect structure in accordance with Claim 2 wherein:

the plurality of interconnected nodes includes a fourth node [[B]] distinct from the first, second, and third nodes ~~A, E and F~~, the fourth node [[B]] having a plurality of data input ports, a plurality of data output ports, and a control signal output port; and

a logic associated with fourth node [[B]] included as part of the routing logic being capable of sending a first control signal [[z]] to the first node [[A]], the first control signal [[z]] containing information concerning routing possibilities through the fourth, third and second nodes ~~B, F and E~~, and the logic associated with the first node [[A]] for routing of data through the first node [[A]] depending at least in part on information concerning routing of data through the fourth, third and second nodes ~~B, F and E~~.

4. (Currently Amended) An interconnect structure in accordance with Claim 3 wherein:

the plurality of interconnected nodes including a fifth node [[C]] distinct from the first, fourth, second, and third nodes ~~A, B, E, and F~~, the fifth node [[C]] having a plurality of data input ports, and a plurality of data output ports;

the fourth node [[B]] sends a message to the fifth node [[C]];

the second node [[E]] sends a second control signal [[y]] to the fourth node [[B]];

the third node [[F]] sends a third control signal [[x]] to the fourth node [[B]];

the logic associated with the fourth node [[B]] sends a non-blocking first control signal [[z]] to the first node [[A]] based on the third and second control signals ~~x and y~~;

the first node [[A]] sends a message to the fifth node [[C]]; and

the fifth node [[C]] simultaneously receives messages into all of its input ports.

5. (Currently Amended) An interconnect structure comprising:

a plurality of nodes including distinct first, second, and third nodes ~~A, B and C~~, the first and second nodes ~~A and B~~ being both positioned to send data to the third node [[C]];

a plurality of interconnect lines selectively coupling the nodes of the interconnect structure;

a control signal carrying line connected from the second node [[B]] to the first node [[A]] for carrying control signals from the second node [[B]] to the first node [[A]]; and

a routing logic associated with the second node [[B]] capable of sending data to the third node [[C]] and sending a control signal to the first node [[A]] that can inform the first node [[A]] that the first node [[A]] is allowed to send a message to the third node [[C]] ;

wherein at least one of the plurality of nodes is adapted to simultaneously receive a plurality of messages.

6. (Currently Amended) An interconnect structure in accordance with Claim 5 wherein:

the third node [[C]] has a plurality of input ports; and

data from the first and second nodes ~~A and B~~ arrive at the third node [[C]] concurrently so that all [[N]] of the input ports of the third node [[C]] receive messages simultaneously.

7. (Currently Amended) An interconnect structure in accordance with Claim 6 wherein:

the plurality of nodes includes distinct first, second, third, fourth, fifth, sixth, and seventh nodes ~~A, B, C, D, E, F and H~~; and

the third node [[C]] is capable of simultaneously sending data from the first node [[A]] to the fourth node [[D]], and capable of sending data form the second node [[B]] to the seventh node [[H]].

8. (Currently Amended) An interconnect structure in accordance with Claim 7 wherein:

the interconnect structure is hierarchical;

the first node [[A]] is on a level of the hierarchy;

the second, third, fourth, and fifth nodes ~~E, B, C, and D~~ are on the level of the hierarchy directly below the level of the first node [[A]]; and

the sixth and seventh nodes ~~F and H~~ are on a level of the hierarchy directly below the level of the second node [[B]].

9. (Currently Amended) An interconnect structure comprising:

a plurality of nodes adapted to generate control signals including the distinct first, second, and third nodes ~~A, B, and C~~, and a collection of interconnect lines selectively coupling the nodes;

the third node [[C]] having a plurality of message input ports, the first and second nodes ~~A and C~~ positioned in the structure so that the first node [[A]] can route a data packet to the third node [[C]];

the second and third nodes ~~B and C~~ positioned in the structure so that the second node [[B]] can route a data packet to the third node [[C]];

the first and second nodes ~~A and B~~ positioned in the network so that the second node [[B]] can send a control signal to the first node [[A]];

a routing logic at the first node [[A]] using the control signal from the second node [[B]] to route messages;

the second node [[B]] routing a first message [[MB]] to the third node [[C]];

the first node A routing a second message [[MA]] to the third node [[C]] to arrive at concurrently with the first message [[MB]];

all input ports of the fifth node [[C]] concurrently receiving a message.

10. (Canceled)

11. (Currently Amended) An interconnect structure in accordance with claim 16, wherein said routing logic assumes that the first message [[MB]] is not blocked from using the first output port and the second message [[MA]] is not blocked from using the second output port.

12. (Currently Amended) An interconnect structure in accordance with claim 11, wherein said routing logic for the routing of the first and second messages ~~MA and MB~~ depends in part on QOS criteria.

13. (Currently Amended) An interconnect structure comprising:

a plurality of interconnected nodes including the first, second, third, fourth, and fifth nodes ~~A, B, C, D, and H~~, each of the first, second, third, fourth, and fifth nodes ~~A, B, C, D and H~~ having a plurality of input ports and a plurality of output ports, and third node [[C]] being positioned to receive messages from the first and second nodes ~~A and B~~ and to route messages to the fourth and fifth nodes ~~D and H~~;

a plurality of interconnect structure output ports including an output port that is accessible from the third node [[C]] but not the fifth node [[H]];

a routing logic included within the interconnect structure to assure that when the first node [[A]] sends a first message [[MA]] to the third node [[C]] and concurrently the second node [[B]] sends a second message [[MB]] to the third node [[C]], then the third node [[C]] can route a first message [[MA]] through the fourth node [[D]] to a target interconnect structure output port for a first message [[MA]] and the third node [[C]] can route a second message [[MB]] through the fifth node [[H]] to a target interconnect structure output port for the second message [[MB]] ;

wherein at least one of the plurality of nodes is adapted to simultaneously receive a plurality of messages.

14. (Currently Amended) An interconnect structure in accordance with claim 13, wherein said routing logic assures that a second message [[MB]] is not blocked from the fifth node [[H]], and a first message [[MA]] is not blocked from the seventh node [[D]].

15. (Original) An interconnect structure in accordance with claim 14, wherein said routing logic is responsive to QOS criteria.

16. (Currently Amended) An interconnect structure comprising:

a plurality of interconnected nodes including a first node [[C]] having first and second input ports ~~I_A and I_B~~ and first and second output ports ~~O_H and O_D~~;

all output ports accessible from first input port [[I_A]] being accessible from output the second output port [[O_D]];

a plurality of output ports that are accessible from the second input port [[I_B]] but not from the first output port [[O_H]]; and

a routing logic included within the interconnect structure to assure that when a second message [[M_A]] arrives at the first input port [[I_A]] and simultaneously the

first [[a]] message [[M_B]] arrives at the second input port [[I_B]] there is a path through the second output port [[O_D]] to a target destination for the first message [[M_B]] ;

wherein at least one of the plurality of nodes is adapted to simultaneously receive a plurality of messages.

17. (Currently Amended) An interconnect structure for carrying message packets consisting of a header and a payload with header indicating a target output port comprising:

a plurality of interconnected nodes including a first node [[C]] having first and second input ports ~~I_A and~~ I_B and first and second output ports ~~O_H and O_D~~;

a plurality of output ports that are accessible from the first input port [[I_B]] but not from the first output port [[O_H]]; and

a routing logic included within the interconnect structure to assure that when a first message [[M_A]] arrives at the first input port [[I_A]] and simultaneously a second message [[M_B]] arrives at a second input port [[I_B]] there is a path through the second output port [[O_D]] to a target destination for the second message [[M_B]] and a path through the first output port [[O_H]] to a target destination for the second message [[M_B]].

18. (Currently Amended) An interconnect structure in accordance with claim 17, wherein said routing logic assumes that a second message [[MB]] is not blocked from using the first output port and a first message [[MA]] is not blocked from using the second output port.

19. (New) An interconnect structure in accordance with Claim 1 wherein:

a plurality of messages simultaneously enter a third node.

20. (New) An interconnect structure in accordance with Claim 19 wherein:

one of the plurality of messages simultaneously entering the third node is sent to a fourth node on the same level as the third node and another of the multiple

messages simultaneously entering the third node is sent to a fifth node on a level below the third node.